

**IN THE CLAIMS:**

We claim:

1           1.     A hybrid substrate comprising:  
2           a substrate having a plurality of pockets patterned thereon; and  
3           at least two different materials provided within a respective pocket of the plurality of  
4           pockets.

1           2.     The hybrid substrate according to Claim 1, wherein the at least two different  
2           materials are approximately co-planar with a top surface of the substrate.

3           3.     The hybrid substrate according to Claim 1, wherein the at least two different  
4           materials are bonded to the substrate.

1           4.     The hybrid substrate according to Claim 1, wherein each of the at least two  
2           different materials is selected from the group consisting of GaAs, InP, silicon wafer, GaN-  
3           based high-electron mobility transistors (HEMTs), and optoelectronic devices.

1           5.     The hybrid substrate according to Claim 1, wherein the substrate is selected  
2           from the group consisting of AlN, quartz, glass, ceramic, CVD diamond, and sapphire.

1           6.     The hybrid substrate according to Claim 1, wherein the substrate is a high  
2           thermal conductive substrate.

1           7.     The hybrid substrate according to Claim 1, wherein each of the plurality of  
2           pockets has a greater surface area than a cross-section surface area of the at least two  
3           different materials.

1           8.     A method for fabricating a hybrid substrate comprising the steps of:  
2           patterning a substrate with a plurality of pockets; and  
3           providing a material within each of the plurality of pockets, wherein at least two  
4           materials provided within two respective pockets of the plurality of pockets are different.

1           9.     The method according to Claim 8, further comprising the step of planarizing  
2           the materials provided within each of the plurality of pockets, such that a top surface of the  
3           materials is approximately co-planar with a top surface of the substrate.

1           10.    The method according to Claim 9, wherein the planarizing step includes a  
2           chem-mech polishing step.

1           11.    The method according to Claim 8, further comprising the step of providing a  
2           thermal conductivity layer between the substrate and the material provided within each of the  
3           plurality of pockets.

1           12.    The method according to Claim 10, wherein the thermal conductivity layer is  
2           a CVD diamond layer.

1           13.    The method according to Claim 8, further comprising the step of providing a  
2           layer of oxide over the material provided within each of the plurality of pockets.

1           14.    The method according to Claim 13, wherein the layer of oxide is a layer of  
2           CVD oxide.

1           15.    The method according to Claim 8, further comprising the step of providing an  
2           oxide on at least one surface of each material before the step of providing the material within  
3           each of the plurality of pockets.

1           16.    The method according to Claim 8, further comprising the step of annealing to  
2           adhere the material provided within each of the plurality of pockets to the substrate.

1           17.     The method according to Claim 8, further comprising the step of preparing the  
2 material provided within each of the plurality of pockets with the blister separation method.

1           18.     The method according to Claim 8, further comprising the step of applying  
2 interconnect structures between the materials provided within the plurality of pockets.

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